REMARKS

Claims 1-13 are pending in the application. Claims 1-13 are rejected.

Claim Amendments

Claims 1, 2 and 5 are amended by rephrasing the term 'capable of' with the term 'for'. Moreover, Claim 3 has been cancelled after fully adding its limitations to Claim 1. Claim 7 has been amended into dependent form, being dependent on Claim 1. Claims 8-13 have been cancelled without prejudice. No new subject matter has been entered through the above amendments.

Claim Rejections

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Settle et al. (US 6,233,253 B1) in view of Hong et al. (US 7,106,757 B2). Applicant respectfully disagrees based on the reasons described as follows.

As indicated in the Office Action, Applicant notes that Settle et al. have taught that "*Further, the functions of the elements of FIG. 6 architecture and the process step in FIG. 1 may be implemented in whole or in part in hardware or within the programmed instructions of a microprocessor such as processor 102 of FIG. 6.*" (See Col. 13, lines 37-41.) But, except for vague and general descriptions, applicant cannot find further disclosure provided by Settle et al. for teaching a transmission circuit in bit level for converting input data of a first rate into output data of a second rate (e.g. putting an operating circuit between input bits and output bits). Moreover, Settle et al. teach using a FIFO (First-In First Out) memory 128 to perform data rate conversion so that "*Data enters the FIFO at the data transfer rate of the internal PC bus 110 and data leaves the*

FIFO 128 at the data of the multiplexed packet stream being generated." (See Col. 8, lines 39-44). To allow for input data and output data to have different transfer rates, Settle et al. teach using an "*oscillator 132 on the board*" to control the FIFO 128. (See Col. 8, lines 44-46). Under the disclosure of Settle et al, persons skilled in the art know how to implement a FIFO, a processor or other elements in whole or in part in hardware or within the programmed instructions of a microprocessor. But, Settle et al. **do not teach persons skilled in the art to change bits of the input data** in the FIFO 128, but teach persons skilled in the art to control output rate with a clock circuit, e.g. the oscillator 132, according to clock information, e.g. DTS(Decoding Time Stamp) or PTS(Presentation Time Stamp), transmitted with video stream. (See Col. 5, lines 47-66.)

In contrast, amended Claim 1 of the present application recites "*a plurality of input units each for receiving one bit of the first data,*" "*a plurality of output units each for outputting one bit of the second data after receiving the bit*" and "***a bit control circuit...without having the bit passing through other input and output units, a number of bits** between the bit received by the input unit and a most significant bit of the **first data being different from a number of bits** between the bit outputted by the output unit and a most significant bit of the **second data***" and "*the bit control circuit further comprises **an operating circuit** electrically connected between the input units and the output units for performing a logical operation according to a predetermined law on the bits received by the input units to generate the bits transmitted by the output units.*" That is, amended Claim 1 seeks protection of a transmission circuit with bit control circuit having an operating circuit between input bits and output bits to perform bit level operation so as to convert input data to output data with different data rates. However, these features are not taught by Settle et al.

Neither Hong et al. teach features of a transmission circuit with **bit control circuits** having **an operating circuit inside** between input bits and output bits so as to convert

input data to output data with different data rates. Applicant notes, as indicated in the Office Action, that "*The enhancement layers are ordered in such a way that the first enhancement layer would contain the most significant bits, and so on. This means that the most significant correction would be made by the first enhancement layer. Combining more enhancement layers would continue to improve the output quality. In this way, the quality of the output video can be "scaled" by combining different numbers of enhancement layers with the base layer.*" (See Col. 4, lines 27-34). Under such circumstances, persons skilled in the art typically convert an image into different layers and put most important information (e.g. the most significant bits) in the first layer. This is called progressive coding (See Col.3, lines 37-43). The features above that are not taught by Settle et al., are also not taught by Hong et al. Therefore, combining the teachings of Settle et al. with Hong et al. would not teach every feature of amended Claim 1 of the present invention.

Moreover, there is no proper motivation to combine the teachings of Settle et al. with Hong et al. Hong describes a software method for streaming multimedia packets over a network, including a Link Layer 106 and a transport layer 104 that are "mostly implemented in host software" (see Col 5 lines 20-45). Hong teaches "implementation of the protocol at the transport layer is preferred" where "The transport layer 104 is responsible of packetizing (emphasis added) data into coding units" (Col 5 lines 42-45). However, Settle teaches a hardware "encoder system 10 for formatting, packetizing, and multiplexing data from a satellite and a DVHS source" (Col 4 lines 30-32). As shown in Fig. 2, "MPEG compatible packets" and "produced by units 18a, 18b, and 18c" (Col 4 lines 56-58). A combination of the above teachings would be detrimental to the performance of Settles' system, as it is designed to alleviate the processor 102 from packetizing duties in order to focus its resources on other peripheral tasks. Forcing the processor 102 to perform packetizing through a software transport layer would therefore

place an additional burden on the processor 102 and reduce/slow its system performance. Therefore, there would be no proper motivation to combine the two respective teachings.

Therefore, for at least these reasons, applicant asserts that the rejection above should be withdrawn, and that amended Claim 1 should be allowed. In addition, amended Claims 2-7 depend from Claim 1 and add further features and are also different and non-obvious with respect to the teachings of Settle et al. and Hong et al.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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